Claims

[c1] What is claimed is:

1.A method of fabricating a memory device on a semiconductor substrate, the surface of the semiconductor substrate comprising a stacked gate, a source and a drain positioned within the semiconductor substrate on either side of the stacked gate, the method comprising:

forming a blocking layer on the semiconductor substrate to cover the stacked gate, the source and the drain;

forming a gettering layer on the blocking layer;

planarizing the gettering layer down to a predetermined thickness;

forming a first barrier layer on the gettering layer;

forming a contact hole, the contact hole penetrating through the first barrier layer, the gettering layer and the blocking layer down to the surface of the source, the drain or the stacked gate;

forming a second barrier layer to cover the first barrier layer and the contact hole; and

etching back the second barrier layer to form a barrier spacer on the side wall of the contact hole.

[c2] 2.The method of claim 1 wherein the first barrier layer or the second barrier layer comprises silicon oxy-nitride or silicon nitride.

[c3] 3.The method of claim 1 wherein a thickness of the first barrier layer ranges from 300 to 1000 angstroms (Å).

[c4] 4.The method of claim 1 wherein a refraction index (RI) of 248nm UV light on the first barrier layer or the second barrier layer ranges from 2 to 2.4.

[c5] 5.The method of claim 1 wherein a dielectric constant (k) of the first barrier layer or the second barrier layer ranges from 0.4 to 0.6.

[c6] 6.The method of claim 1 wherein a thickness of the second barrier layer ranges from 100 to 350 Å .

[c7] 7.The method of claim 1 wherein the stacked gate comprises a floating gate, an ONO dielectric layer positioned on the floating gate, and a control gate

positioned on the ONO dielectric layer.

[c8] 8.The method of claim 1 wherein a thickness of the gettering layer ranges from 13K to 15K Å .

[c9] 9.The method of claim 1 wherein the gettering layer comprises PSG or BPSG.

[c10] 10.The method of claim 1 wherein the predetermined thickness ranges from 7K to 9K Å .

[c11] 11.The method of claim 1 wherein the semiconductor substrate is a silicon substrate.

[c12] 12.The method of claim 1 wherein after the second barrier layer is etched back, the method further comprises:

forming an adhesive layer on the surfaces of the first barrier layer and the barrier spacer;

performing a contact plug process to fill a metal material within the contact hole; and

etching back the metal material to form a contact plug within the contact hole.

[c13] 13.The method of claim 12 wherein the metal material is tungsten (W).

[c14] 14.The method of claim 1 wherein the first barrier layer is 10% to 50% thicker than the second barrier layer.

[c15] 15.The method of claim 1 wherein the blocking layer is at least one selected from the group consisting of undoped silicate glass (USG), LP-TEOS, and PE-TEOS.

[c16] 16.The method of claim 1 wherein after the second barrier layer is etched back, the method further comprises:

forming an adhesive layer on the surfaces of the first barrier layer and the barrier spacer;

performing a contact plug process to fill a metal material within the contact hole; and

etching back the metal material, the adhesive layer and the second barrier layer

to form a contact plug within the contact hole.

[c17] 17.The method of claim 16 wherein the metal material is tungsten (W).